Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claim 1 (currently amended): A semiconductor device in chip format, comprising:

a chip;

electrical connection pads disposed on said chip;

~~at least one first insulating~~ a first passivation layer disposed on said chip such that said electrical connection pads are free of said first ~~insulating~~ passivation layer on at least one surface;

interconnects running on said first ~~insulating~~ passivation layer and in each case ~~lead~~ leading from said electrical connection pads to base regions;

a second passivation layer disposed on said interconnects and on said first passivation layer, said second passivation layer having openings formed therein leading to said base regions;

~~a second~~ at least one insulating layer disposed on said interconnects and on said ~~first insulating~~ second passivation layer, said ~~second~~ at least one insulating layer having a

layer thickness, said ~~second~~ at least one insulating layer having openings formed therein leading to said base regions;

cylinders of a conductive material with an elasticity, ~~introduced into~~ disposed in each of said openings;

small balls disposed on said cylinders of said conductive material in a region of a free end of each of said openings, said small balls having an elasticity and being metallic at least on an outside; ~~and~~

said at least one insulating layer being at least four times thicker than said first passivation layer; and

said thickness of said ~~second~~ insulating layer, said elasticity of said conductive material, and said elasticity of said small balls being selected for obtaining a desired level of comparatively good mechanical decoupling from a printed circuit board upon the semiconductor component being soldered onto the printed circuit board.

Claim 2 (cancelled).

Claim 3 (currently amended): A method for producing semiconductor devices in a chip format, which comprises:

providing chips;

placing electrical connection pads on the chips;

applying ~~at least one first insulating~~ a first passivation layer to at least one surface of the chips such that the electrical connection pads are left at least partially uncovered by the first ~~insulating~~ passivation layer;

producing interconnects on the ~~at least one first insulating~~ first passivation layer, the interconnects leading to base regions of external connection elements;

applying a second passivation layer on the interconnects and on the first passivation layer;

applying ~~a second~~ at least one insulating layer on the interconnects and on the ~~at least one first insulating~~ second passivation layer, the ~~second~~ at least one insulating layer having a thickness at least four times thicker than the first passivation layer;

forming openings in the ~~second~~ at least one insulating layer above the base regions and leading to the base regions;

introducing cylinders of a conductive material with an elasticity into the openings;

placing small balls onto the cylinders of the conductive material in a region of a free end of each of the openings, said small balls having an elasticity and being metallic at least on an outside; and

selecting the thickness of ~~said second~~ the at least one insulating layer, the elasticity of the conductive material, and the elasticity of the small balls to obtain a desired level of comparatively good mechanical decoupling from a printed circuit board upon the semiconductor component being soldered onto the printed circuit board.

Claim 4 (previously presented): The method according to claim 3, which comprises using a doctor blade for introducing the conductive material into the openings.

Claim 5 (previously presented): The method according to claim 19, which comprises

forming the chips on a wafer; and

after the curing of the conductive adhesive, dividing the wafer to obtain the semiconductor devices.

Claims 6-10 (canceled).

Claim 11 (withdrawn): The method according to claim 18, which comprises:

forming the chips on a wafer; and

after the remelting of the solder paste, dividing the wafer to obtain the semiconductor devices.

Claim 12 (withdrawn): The semiconductor device according to claim 1, wherein said conductive material is a solder paste which has been remelted after introduction into said opening.

Claim 13 (previously presented): The semiconductor device according to claim 1, wherein said conductive material is a conductive adhesive which has been cured after introduction into said opening.

Claim 14 (previously presented): The semiconductor device according to claim 13, wherein said small balls are composed completely of metal.

Claim 15 (previously presented): The semiconductor device according to claim 1, wherein said small balls are metallized plastic balls.

Claim 16 (cancelled).

Claim 17 (currently amended): The semiconductor device according to claim 1, wherein said second ~~insulating~~ passivation layer is thicker than said first ~~insulating~~ passivation layer.

Claim 18 (withdrawn): The method according to claim 3, wherein the conductive material introduced into the opening is a solder paste which has been remelted after introduction into said opening.

Claim 19 (previously presented): The method according to claim 3, wherein the conductive material introduced into the opening is a conductive adhesive which has been cured after introduction into the opening.

Claim 20 (previously presented): The method according to claim 19, wherein the small balls disposed on the conductive adhesive are composed completely of metal.

Claim 21 (previously presented): The method according to claim 3, wherein the small balls disposed on the conductive material are metallized plastic balls.

Claim 22 (cancelled).

Claim 23 (currently amended): The method according to claim 3, wherein the applied second ~~insulating~~ passivation layer is thicker than the applied first ~~insulating~~ passivation layer.

Claims 24-25 (cancelled).